Remarks

Applicant respectfully requests that the above amendments be entered under 37 C.F.R. § 1.116 because they are believed to place the claims in better condition for consideration on appeal. Claims 19, 28 and 35 have been amended. No claims have been canceled. Therefore, claims 19-37 are now presented for examination.

In the Final Office Action, claims 19-22, 24-31 and 33-36 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Anderson, U.S. Patent No. 5,905,910 ("Anderson"), and Jones et al., U.S. Patent No. 5,619,723 ("Jones")/Labatte et al., U.S. Patent No. 5,913,0575 ("Labatte").

Applicant submits that Labatte may not be considered as prior art precluding patentability of the present invention. Section 103(c) of Title 35 of the United States Code was amended in November 1999 to include references which qualify as prior art under 35 U.S.C §102(e). Section 103(c) currently reads:

> *Subject matter developed by another person, which qualifies as prior art only under one or more of the subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.*

Labatte is considered prior art under 35 U.S.C. §102(e) because it was filed before the present application, but issued after the filing of the application (effective filing date: 10-01-1998). Additionally, at the time of conception of the claimed invention, the cited reference, as well as the claimed invention was subject to an obligation of assignment to Intel Corporation. Therefore, due to the §102(e) status of the cited reference, and in light of §103(c), Labatte cannot be used as a reference to preclude patentability of claims 19-22, 24-31 and 33-36 under 35 U.S.C §103.

Moreover, the present claims are patentable over the combination of Anderson and Jones. Anderson discloses a system for the simultaneous operation of multiple disk drives in a computer. The system includes a first disk drive having an interrupt generating circuit to generate a first interrupt signal. The first disk drive receives a first disk transfer command from the computer, processes the first disk transfer command, and generates the first interrupt signal upon completion of the first disk data transfer command.

The system also includes a second disk drive, also having an interrupt generating circuit to generate a second interrupt signal. The second disk drive receives a second disk transfer command from the computer while the first disk drive is processing the first disk transfer command such that both the first and second disk drives are simultaneously active. The second disk drive processes the second disk transfer command and generates the second interrupt signal upon completion of the second disk data transfer command. See Anderson at col. 1 ll. 49-65.

Nevertheless, Anderson does not disclose or suggest an interface coupled to a system bus that receives drive requests from a BIOS via a system bus. In fact, the Office Action admits that Anderson fails to teach an interface that is connected to a system bus and communicates with BIOS. See Final Office Action at page 3 lines 13-17.

Jones discloses a disk drive array controller. The controller includes a microcontroller CPU with embedded ROM and RAM, a bus interface, and five connected disk drives. The ROM 104 contains the firmware for controller. A system bus coupled to the bus interface provides a communication link between the controller and a host computer, which uses the array of disk drives as secondary memory. See Jones at col. 14, ll. 18-27. When the host sends a read or write request to the array via the system bus, the interface translates the request to the controller, which generates access requests for each of the individual disk drives col. 15, ll. 10-15).

Applicant submits that Jones does not disclose or suggest an interface coupled to a system bus that receives drive requests from a BIOS via a system bus. However, the Examiner asserts that:

> Jones discloses an interface connected to a system bus and that communicates with BIOS.

(Office Action at page 3 lines 18-19).

Applicant disagrees with the Examiner's assertion. Jones discloses a microcontroller CPU having an integrated ROM that includes firmware. The CPU is coupled to a bus interface, which is in turn coupled to a bus interface. There is no disclosure or suggestion, however, of the interface communicating with BIOS.

Notwithstanding the Examiner's assertion, Jones still does not disclose or suggest an interface coupled to a system bus that receives drive requests from BIOS via a system bus. Assuming that the Examiner's interpretation of the Jones reference is correct, an interface connected to a system bus and communicates with BIOS is not analogous to an interface coupled to a system bus that receives drive requests from a BIOS via the system bus.

Claim 19 recites an interface coupled to a system bus that receives disk drive requests from a Basic Input Output System (BIOS) via the system bus. As described above, neither Anderson nor Jones recite an interface coupled to a system bus that receives disk drive requests from BIOS via a system bus. Thus, since neither Anderson nor Jones recite such a limitation, any combination of Anderson and Jones would also not disclose or suggest an interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. Therefore, claim 19 is patentable over the combination of Anderson and Jones.

Claims 20-24 depend from claim 19 and include additional limitations. As a result, claims 20-24 are also patentable over the combination of Anderson and Jones.

Claim 25 recites receiving an IDE request from a Basic Input Output System (BIOS) at an IDE interface via a system bus. Therefore, for the reasons stated above with respect to claim 19, claim 25 is also patentable over the combination of Anderson and Jones. Since claims 26 and 27 depend from claim 25 and include additional limitations, claims 26 and 27 are also patentable over the combination of Anderson and Jones.

Claim 28 recites an interface coupled to a system bus that receives disk drive requests from a Basic Input Output System (BIOS) via the system bus. Accordingly, for the reasons stated above with respect to claim 19, claim 28 is also patentable over the combination of Anderson and Jones. Because claims 29-34 depend from claim 28 and include additional limitations, claims 29-34 are also patentable over the combination of Anderson and Jones.

Claim 35 recites an IDE interface coupled to the system bus that receives IDE requests from a Basic Input Output System (BIOS) via the system bus. Thus, for the reasons stated above with respect to claim 19, claim 35 is also patentable over the combination of Anderson and Jones. Since claims 36 and 37 depend from claim 35 and include additional limitations, claims 36 and 37 are also patentable over the combination of Anderson and Jones.

Claims 23 and 32 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Anderson, Jones/Labatte and further in view of Jenkins, U.S. Patent No. 4,047,157 ("Jenkins"). As described above, Labatte cannot be used as a reference to preclude patentability of claims 23 and 32 under 35 U.S.C §103.

Further, applicant submits that the present claims are patentable over Anderson and Jones even in view of Jenkins. Jenkins discloses a controller in a secondary storage facility that can transfer data from a recording medium over either of two independent buses in a data system. See Jenkins at col. 2, ll. 36-40. Nevertheless, Jenkins does not disclose or suggest an interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. As described above, neither Anderson nor Jones

disclose or suggest such a limitation. Therefore, the present claims are patentable in view of any combination of Anderson, Jones and Jenkins since none of the references disclose or suggest an interface coupled to a system bus that receives disk drive requests from a BIOS via a system bus.

Claim 37 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson and Jones/Labatte and further in view of Mizuno et al., U.S. Patent No. 5,608,891 ("Mizuno"). As discussed above, Labatte cannot be used as a reference to preclude patentability of claim 37 under 35 U.S.C §103. In addition, applicant submits that the present claims are patentable over Anderson and Jones even in view of Mizuno.

Mizuno discloses an array type recording system that divides a single circuit into a write circuit and a read circuit. See Mizuno at col. 4, ll. 30-35. However, Mizuno does not disclose or suggest an interface coupled to a system bus that receives disk drive requests from a BIOS via the system bus. As described above, neither Anderson nor Jones disclose or suggest such a limitation. Therefore, the present claims are patentable over any combination of Anderson, Jones and Mizuno.

Applicant respectfully submits that the rejections have been overcome by the amendments and remarks, and that the claims as amended are now in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims as amended be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 4/10/02

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Version with Markings to Show Changes Made
Insertions are underlined, deletions are bracketed.

19. (Twice Amended) A system comprising:

an interface coupled to a system bus that receives disk drive requests from a Basic Input Output System (BIOS) via the system bus;

a first disk drive;

a second disk drive, the first and second disk drives each having data separator electronics, data formatting electronics and head positioning electronics; and

a striping controller coupled between the interface and the first and second disk drives, that causes data being transmitted between the system bus and the first and second drives to be written to and read from the first and second drives in an interleaved form and substantially in parallel.

28. (Twice Amended) A striping disk controller comprising:

an interface coupled to a system bus that receives disk drive requests from a Basic Input Output System (BIOS) via the system bus; and

control logic coupled to the interface to cause data being transmitted via the system bus to be written to and read from a first disk drive and a second disk drive in an interleaved form and substantially in parallel.

35. (Twice Amended) A system comprising:

a central processing unit (CPU) that executes an operating system including a Basic Input/Output Operating System (BIOS);

a system bus coupled to the CPU;

an IDE interface coupled to the system bus that IDE drive receives requests from a Basic Input Output System (BIOS) via the system bus;

a striping controller coupled to the IDE interface;

a first storage device coupled to the striping controller; and

a second storage device coupled to the striping controller;

the striping controller, based on a standard IDE driver instruction, causes data being received to be written to and read from the first and second storage devices in an interleaved form and substantially in parallel.